Amendments to the Specification:

Please amend the paragraph beginning at line 3 on page 1 as follows:

This application claims priority under 35 U.S.C. 120 as a continuation-in-part of U.S. Patent Application Serial No. 09/534,838, entitled "Bandwidth Division for Packet Processing," filed March 24, 2000, to Dyckerhoff et al., and U.S. Patent Application Serial No. [[_____]] 09/751,454 (attorney docket no. 0023-0014), entitled "Bandwidth Division for Packet Processing," filed January 2, 2001, to Dyckerhoff et al. The contents of both applications are hereby incorporated by reference.

Please amend the paragraph beginning at line 13 on page 6 as follows:

As shown in Fig. 3, I/O board 230A includes receiver module 310A, transmitter module 310B, framer/deframer module 330, sprayer module 340, desprayer module 350, a plurality of preprocessing modules 360A-360D, and a plurality of corresponding RAMs 370A-370D. Receiver module 310A and transmitter module 310B connect to framer/deframer module 330. Sprayer module 340 and desprayer module 350 connect to framer/deframer module 330 and to each of the preprocessing modules 360A-360D. Each of the preprocessing modules 360A-360D connect to respective RAMs 370A-370D and connect to respective switching/forwarding modules. In a preferred embodiment, each of the components and modules of I/O board 230A is integrated on a separate chip/module and the chips/modules are mounted on a single board. Alternatively, the components and modules may be all integrated onto a single chip. In other embodiments, the functionality of the components and modules may all be integrated on one or more chips, which are mounted on one or more separate boards.

Please amend the paragraph beginning at line 18 on page 7 as follows:

Framer/deframer module 330 operates as a framer to extract data packets from an in-coming stream of data and as a deframer to form an out-going stream of data from data packets.

Please amend the paragraph beginning at line 20 on page 7 as follows:

As a framer for in-coming data, framer/deframer module 330 receives an in-coming stream of data from receiver module 310A. The in-coming stream of data received by framer/deframer module 330 may be a single stream of data or may be multiple streams of data (e.g., 16 streams from receiver module 310A, as described in the above example). Framer/deframer module 330 deserializes the in-coming stream of data (i.e., forms multiple parallel streams from a single stream or forms additional parallel streams from multiple streams). Framer/deframer module 330 preferably has a multi-line internal bus corresponding to the number of streams to which the data has been deserialized. For example, framer/deframer module 330 converts 16 streams of data clocked at 622MHz to 128 streams of data clocked at 77 MHz. In this example, framer/deframer module 330 preferably has a 128-line bus for extracting data packets from the 128 streams of data. In one embodiment, to extract data packets, framer/deframer module 330 may perform framing (such as SONET framing to identify the beginning and end of the packets) and other processing to prepare the data packets, such as removing link layer overhead (such as SONET and HDLC overhead), descrambling, and error checking.

Please amend the paragraph beginning at line 12 on page 8 as follows:

As a deframer for out-going data, framer/deframer module 330 receives data packets and forms an out-going data stream. In a preferred embodiment, framer/deframer module 330 has a multi-line bus for processing the received data packets (e.g., 128-line bus). Framer/deframer module 330 identifies the beginning and end of data packets and processes the packets for transmission on an external communication link. Such processing may include adding appropriate link layer overhead (such as SONET and HDLC overhead), performing error detection calculations, and scrambling. Framer/deframer module 330 also serializes the data to form an out-going data stream. The out-going data stream may be a single stream of data or may be multiple streams of data (e.g., 16 streams for the transmitter module 310B, as described in the above example). In one embodiment, framer/deframer module 330 receives data packets on a 128-line bus clocked at 77MHz, processes the packets for transmission, and converts the data into 16 streams of data clocked at 622MHz.

Please amend the paragraph beginning at line 1 on page 9 as follows:

Examples of implementations of a framer/deframer ~~and deframer~~ module 330 are described in U.S. Patent Application No. 09/637,709, entitled "Systems and Method For Packing Data into a Data Register," filed August 15, 2000, to Padmanabhan et al. and U.S. Patent Application No. 09/706,752, entitled "Systems and Methods for Generating a Reliable Clock for Reception and Data Recovery," filed November 7, 2000, to Padmanabhan et al. The contents of both applications are hereby incorporated by reference.

Please amend the paragraph beginning at line 7 on page 9 as follows:

Sprayer module 340 receives data packets from framer/deframer module 330 and transmits them across a plurality of data paths. In a preferred embodiment, sprayer module 340 contains a plurality of output channels or outputs, each coupled to one of the plurality of data paths to a switching/routing module. There are various ways that sprayer module 340 may select the data path on which each data packet is sent. For example, sprayer module 340 may use a predetermined hash algorithm, a fixed pattern, randomly, or based on some mechanism for load balancing. Sprayer module 340 preferably includes a mechanism, such as injecting delay or packet tagging, to avoid reordering of data packets as they emerge from their respective data paths. In one embodiment, sprayer module 340 receives data packets from a single framer/deframer module across a multi-line bus (e.g., 128-line bus). In other embodiments, sprayer module 340 receives data packets from a plurality of framer/deframer modules, in which case bus lines are preferably allocated to each framer/deframer module for receiving data packets.

Please amend the paragraph beginning at line 19 on page 9 as follows:

Desprayer 350 receives data packets from multiple data paths (or input channels connected to the data paths). In one embodiment, desprayer 350 combines the data packets received from the plurality of input channels into a single stream on a multi-line bus (e.g., 128-line bus) coupled to framer/deframer module 330.

Please amend the paragraph beginning at line 1 on page 10 as follows:

Examples of implementations of the sprayer module and desprayer module are described

in U.S. Patent Application Serial No. 09/534,838, entitled "Bandwidth Division for Packet Processing," filed March 24, 2000, to Dyckerhoff et al., and U.S. Patent Application Serial No. [[_____]] 09/751,454 (attorney docket no. 0023-0014), entitled "Bandwidth Division for Packet Processing," filed January 2, 2001, to Dyckerhoff et al.

Please amend the paragraph beginning at line 3 on page 11 as follows:

Processing board 410 and line interfaces 420A-420B are shown in greater detail in Fig. 5. The components of processing board 410 are similar to those components shown in Fig. 3 having the same reference numerals. Sprayer module 500 performs similar functions as sprayer module 340, except that sprayer module 500 is connected to more than one ~~frame~~ framer/deframer module. Accordingly, sprayer module 500 preferably allocates a portion of its input lines to receiving data packets from one of the framer/deframer modules (e.g., framer/deframer module 426A) and the remaining input lines to receiving data packets from the other framer/deframer module (e.g., framer/deframer module 426B). While two framer/deframer modules are shown connected to sprayer module 500, more than two framer/deframer modules may be connected. In such a case, the appropriate number of input lines is preferably allocated to each of the connected framer/deframer modules. In addition, sprayer module 500 has logic for determining which data packets to process (e.g., spray) from framer/deframer module 426A and framer/deframer module 426B (or whatever framer/deframer modules are connected to the input of sprayer 500). In one embodiment, sprayer 500 contains a FIFO and data packets received from either framer/deframer module are added to the FIFO. Sprayer 500 processes the data packet that was added to the FIFO earliest.

Please amend the paragraph beginning at line 18 on page 11 as follows:

Similar modifications and adjustments are preferably made to desprayer module 510. For example, desprayer module preferably maintains address information for each of the framer/deframer modules (or line interfaces) connected to desprayer 510. Certain output lines are allocated to each of the connected framer/deframer modules. When desprayer 510 receives data packets, it outputs the data packets to the appropriate framer/deframer module on the corresponding output lines.

Please amend the paragraph beginning at line 8 on page 12 as follows:

Fig. 6 shows a flow diagram of how an in-coming data stream is processed, consistent with the invention. A receiver module receives a single data stream (step 610). The single data stream is deserialized onto a multi-line bus operating at a lower clock speed than the receiver module (step 615). Data packets are extracted from the data carried on the multi-line bus (step 620). The data packets are sprayed across a plurality of data paths for processing. For example, one of a plurality of switching/forwarding modules may be selected for ~~reach~~ each data packet (step 630). For each path selected (steps 640A-640M), the data packets are stored in RAM (steps 650A-650M) and transmitted (or at least a portion of the data packets) to the respective switching/forwarding module (step 660A-660M).

Please amend the paragraph beginning at line 17 on page 12 as follows:

Fig. 7 shows a flow diagram of how an out-going data stream is processed. Data packets

are received from a plurality of switching/forwarding modules (step 710). The data packets are carried on a multi-line bus and processed for link transmission (step 720). The data is serialized to form a single data stream (step 730) and transmitted from the transmitter module to the external communication link (step 740).